WHAT IS CLAIMED IS:

1. A memory array comprising:

a bit cell row comprising a bit cell, the bit cell comprising a first transistor disposed in a first bit cell body region, the first transistor including a first active region;

a strap cell row comprising a strap cell, the strap cell comprising a first strap cell body region conductively coupled to the first bit cell body region;

a first power supply line electrically coupled to the first active region and providing a first supply voltage potential to the first active region; and

a first offset supply line electrically coupled to the first strap cell body region and providing a first offset voltage potential to the first bit cell body region via the first strap cell body region, wherein the first supply voltage potential is operable to be different from the first offset voltage potential.

2. The memory array of Claim 1, wherein the first supply voltage potential is operable to be different from the first offset voltage potential in a standby mode of the bit cell.

3. The memory array of Claim 2, wherein the first supply voltage potential is substantially the same as the first offset voltage potential in an active mode of the bit cell.

4. The memory array of Claim 1, wherein the difference between the first offset voltage potential and the first supply voltage potential is operable to be controlled such that the difference is greater in a standby mode of the bit cell than in an active mode of the bit cell.

5. The memory array of Claim 1, wherein the first transistor is an n-channel transistor, wherein the first bit cell body region is a p-type substrate, wherein the first offset voltage potential is a substrate voltage potential, wherein the first supply voltage potential is a low power supply voltage, and wherein the first supply voltage potential is operable to be greater than the first offset voltage potential.

6. The memory array of Claim 5, wherein the memory array is coupled to a peripheral circuit, wherein the peripheral circuit has a low power supply voltage potential, and wherein the first supply voltage potential of the memory array is operable to be greater than the low power supply voltage potential of the peripheral circuit.

7. The memory array of Claim 1, wherein the first transistor is a p-channel transistor, wherein the first bit cell body region is an n-well region, wherein the first offset voltage potential is an n-well voltage potential, wherein the first supply voltage potential is a high power supply voltage, and wherein the first supply voltage potential is operable to be less than the first offset voltage potential.

8. The memory array of Claim 7, wherein the memory array is a coupled to a peripheral circuit, wherein the peripheral circuit has a high power supply voltage potential, and wherein the first supply voltage potential of the memory array is operable to be less than the high power supply voltage potential of the peripheral circuit.

9. The memory array of Claim 1, wherein the bit cell comprises a bit cell geometry and the strap cell comprises a strap cell geometry substantially similar to the bit cell geometry.

10. The memory array of Claim 1, wherein the bit cell further comprises a second transistor disposed in an n-well region, the n-well region extending generally along a first direction, and wherein the memory array further comprises a bit line electrically coupled to the first transistor and extending generally along the first direction.

11. The memory array of Claim 1, wherein the memory array is a static random access memory array.

12. The memory array of Claim 1, wherein the bit cell is a six-transistor static random access memory cell.

13. The memory array of Claim 1, wherein the memory array further comprises a conductive layer and a word line formed in the conductive layer and electrically coupled to the bit cell, and wherein the first offset supply line is formed in the conductive layer.

14. The memory array of Claim 1, wherein the first supply voltage potential may be controlled separately from the first offset voltage potential.

15. The memory array of Claim 1, wherein the bit cell further comprises a second transistor disposed in a second bit cell body region, the second transistor including a second active region; wherein the strap cell further comprises a second strap cell body region conductively coupled to the second bit cell body region; and wherein the memory array further comprises:

a second power supply line electrically coupled to the second active region and providing a second supply voltage potential to the second active region; and

a second offset supply line electrically coupled to the second strap cell body region and providing a second offset voltage potential to the second bit cell body region via the second strap cell body region, wherein the second supply voltage potential is operable to be different than the second offset voltage potential.

16. The memory array of Claim 15, wherein the first transistor is a p-channel transistor, wherein the first bit cell body region is an n-well region, wherein the first offset voltage potential is an n-well voltage potential, and wherein the first supply voltage potential is operable to be less than the first offset voltage potential; and

wherein the second transistor is an n-channel transistor, wherein the second bit cell body region is a p-type substrate, wherein the second offset voltage potential is a substrate voltage potential, and wherein the second supply voltage potential is operable to be greater than the second offset voltage potential.

17. The memory array of Claim 16, wherein the memory array is a coupled to a peripheral circuit, the peripheral circuit having a low power supply voltage potential and a high power supply voltage potential; and wherein the first offset voltage potential is substantially the same as the high power supply voltage potential of the peripheral circuit and the second offset voltage potential is substantially the same as the low power supply voltage potential of the peripheral circuit.

18. The memory array of Claim 15, wherein the memory array further comprises a first conductive layer, a second conductive layer, and a word line electrically coupled to the bit cell, and wherein the first offset supply line is formed in the first conductive layer and the second offset supply line and the word line are formed in the second conductive layer.

19. The memory array of Claim 18, the memory array further comprises a third conductive layer and a bit line electrically coupled to the bit cell, wherein the first power supply line, the second power supply line, and the bit line are formed in the third conductive layer.

20. A method of reducing memory array leakage current, the method comprising:

providing a memory array comprising a bit cell and a strap cell, wherein the bit cell comprises a first transistor disposed in a first bit cell body region, the first transistor including a first active region, and wherein the strap cell comprises a first strap cell body region conductively coupled to the first bit cell body region;

applying a first supply voltage potential to the first active region; and

applying a first offset voltage potential to the first bit cell body region via the first strap cell body region, wherein the first supply voltage potential is operable to be different from the first offset voltage potential.

21. The method of Claim 20, wherein the first supply voltage potential is operable to be different from the first offset voltage potential in a standby mode of the bit cell.

22. The method of Claim 21, wherein the first supply voltage potential is substantially the same as the first offset voltage potential in an active mode of the bit cell.

23. The method of Claim 20, further comprising controlling the first offset voltage potential such that the difference between the first offset voltage potential and the first supply voltage potential is greater in a standby mode of the bit cell than in an active mode of the bit cell.

24. The method of Claim 20, further comprising controlling the first supply voltage potential such that the difference between first offset voltage potential and the first supply voltage potential is greater in a standby mode of the bit cell than in an active mode of the bit cell.

25. The method of Claim 20, wherein the first transistor is an n-channel transistor, wherein the first bit cell body region is a p-type substrate, wherein the first offset voltage potential is a substrate voltage potential, and wherein the first supply voltage potential is operable to be greater than the first offset voltage potential.

26. The method of Claim 20, wherein the first transistor is a p-channel transistor, wherein the first bit cell body region is an n-well region, wherein the first offset voltage potential is an n-well voltage potential, and wherein the first supply voltage potential is operable to be less than the first offset voltage potential.

27. The method of Claim 20, wherein the bit cell comprises a bit cell geometry and the strap cell comprises a strap cell geometry substantially similar to the bit cell geometry.

28. The method of Claim 20, wherein the memory array is a static random access memory array.

29. The method of Claim 20, wherein the bit cell further comprises a second transistor disposed in a second bit cell body region, the second bit cell including a second active region; wherein the strap cell further comprises a second strap cell body region conductively coupled to the second bit cell body region, and wherein the method further comprises:

applying a second supply voltage potential to the second active region; and

applying a second offset voltage potential to the second body region via the second strap cell body region, wherein the second supply voltage potential is operable to be different than the second offset voltage potential.

30. The method of Claim 29, wherein the first transistor is a p-channel transistor, wherein the first bit cell body region is an n-well region, wherein the first offset voltage potential is an n-well voltage potential, and wherein the first supply voltage potential is operable to be less than the first offset voltage potential; and

wherein the second transistor is an n-channel transistor, wherein the second bit cell body region is a p-type substrate, wherein the second offset voltage potential is a substrate voltage potential, and wherein the second supply voltage potential is operable to be greater than the second offset voltage potential.

31. A memory array strap cell comprising:

a first strap cell body region operable to be coupled to a first bit cell body region of a bit cell comprising a first transistor including a first active region disposed in the first bit cell body region; and

a first conductive contact coupled to the first strap cell body region;

wherein the strap cell is operable to communicate a first offset voltage potential from a first offset supply line to the first bit cell body region via the first conductive contact and the first strap cell body region; and

wherein the first offset voltage potential is operable to be different from a first supply voltage potential received by the first active region from a first power supply line.

32. The strap cell of Claim 31, wherein the first supply voltage potential is operable to be different from the first offset voltage potential in a standby mode of the bit cell.

33. The strap cell of Claim 32, wherein the first supply voltage potential is substantially the same as the first offset voltage potential in an active mode of the bit cell.

34. The strap cell of Claim 31, wherein the difference between the first offset voltage potential and the first supply voltage potential is operable to be controlled such that the difference is greater in a standby mode of the bit cell than in an active mode of the bit cell.

35. The strap cell of Claim 31, wherein the strap cell comprises a strap cell geometry substantially similar to a geometry of the bit cell.

36. The strap cell of Claim 31, wherein the bit cell further comprises a second transistor disposed in an n-well region, the n-well region extending generally along a first direction, and wherein the strap cell further comprises a bit line electrically coupled to the first transistor and extending generally along the first direction.

37. The strap cell of Claim 31, wherein the strap cell is a component of a logic circuit, wherein the logic circuit has a logic circuit supply voltage potential, and wherein the first supply voltage potential is substantially the same as the logic circuit supply voltage potential.

38. The strap cell of Claim 31, further comprising:

a second strap cell body region operable to be coupled to a second bit cell body region of the bit cell, wherein a second transistor including a second active region is disposed in the second bit cell body; and

a second conductive contact coupled to the second strap cell body region;

wherein the strap cell is operable to communicate a second offset voltage potential from a second offset supply line to the second bit cell body region via the second conductive contact and the second strap cell body region; and

wherein the second offset voltage potential is operable to be different from a second supply voltage potential received by the second active region from a second power supply line.

39. The strap cell of Claim 38, wherein the first transistor is a p-channel transistor, wherein the first bit cell body region is an n-well region, wherein the first offset voltage potential is an n-well voltage potential, and wherein the first supply voltage potential is operable to be less than the first offset voltage potential; and

wherein the second transistor is an n-channel transistor, wherein the second bit cell body region is a p-type substrate, wherein the second offset voltage potential is a substrate voltage potential, and wherein the second supply voltage potential is operable to be greater than the second offset voltage potential.